AMENDMENTS TO THE CLAIMS

1–8 (cancelled)

9. (currently amended) A method for performing serial data to parallel data conversion, the method comprising:

serially receiving a data word at a serial data input interface;

providing said received data word to a serial-to-parallel mapping circuit;

partitioning said provided received data word into a plurality of partitioned received data words;

generating memory write control signals and memory write address signals;

directing said generated memory write control signals and said generated memory write address signals to a first port of a dual port memory device;

writing said partitioned provided received data words to a first port of said dual port memory device in response to said directing;

generating memory read control signals and memory read address signals;

directing said memory read control signals and said memory read address signals to a second port of said dual port memory device;

reading an output data word from said second port of said dual port memory device in response to said directing said direct said memory read control signals and said memory read address signals; and

reordering bits of said output data word to provide a parallel output data word.

10. (previously presented) The method of claim 9 wherein said partitioning is performed by said serial-to-parallel mapping circuit.

11. (previously presented) The method of claim 9 wherein said generating said memory write control signals and said memory write address signals is performed by said serial-to-parallel mapping circuit.

12. (cancelled)

13. (previously presented) The method of claim 9 wherein said writing said partitioned provided received data words comprises:

writing said partitioned provided received data words to uniquely associated memory addresses in said memory device.

14. (cancelled)

15. (previously presented) The method of claim 9 wherein said reading an output data word from of said memory device comprises:

reading said output data word with an output mapping circuit.

16. (previously presented) The method of claim 9 wherein said reordering said bits of said output data word comprises:

mapping interconnects between an output port of an output mapping circuit and an input port of a parallel output interface.

17. (previously presented) The method of claim 9 further comprising:

providing a clock rate for said serial-to-parallel mapping circuit which is at least eight times faster than a clock rate for said serial data input interface.

18. (currently amended) A method for conducting parallel data to serial data conversion, the method comprising:

receiving a parallel data word;

reordering at least one bit of said received parallel data word to provide a reordered parallel data word;

writing said reordered parallel data word to a first port of a dual port memory device;

reading output data from a second port of said dual port memory device;

partitioning said read output data into a plurality of serial data words; and

providing a serially converted output data word from said plurality of partitioned serial data words.

19. (previously presented) The method of claim 18 wherein said receiving said parallel data word comprises:

receiving said parallel data word at a parallel-to-serial input mapping circuit.

20. (previously presented) The method of claim 18 wherein said reordering comprises:

reordering said received parallel data word at a parallel-to-serial input mapping circuit.

21–22. (cancelled)

23. (previously presented) The method of claim 18 wherein said reordering comprises:

mapping interconnects between a parallel-to-serial input mapping circuit and said memory device.

24. (currently amended) A method for performing serial data to parallel data conversion, the method comprising:

serially receiving a data word at a serial data input interface;

partitioning said received data word into a plurality of partitioned received data words;

writing said partitioned received data words to a first port of a dual port memory device;

reading an output data word from a second port of said dual port memory device; and

reordering at least one bit of said output data word to provide a parallel output data word.

25. (previously presented) The method of claim 24 wherein said reordering comprises:

mapping interconnects between an output port of an output mapping circuit and an input port of a parallel output interface.

26. (previously presented) The method of claim 24 wherein said reordering comprises:

reordering said at least one bit of said output data word during communication of said output data word between two connected digital logic devices.

27. (previously presented) The method of claim 24 wherein said reordering comprises:

mapping interconnects between two connected digital logic devices.

28. (previously presented) A serial-to-parallel and parallel-to-serial converter comprising:

a serial data input interface for receiving a serial input data word;

an input memory connected to said serial data input interface and responsive to said receiving to convert said serial input data word into a parallel output data word, said input memory including a first memory device having a two memory banks, which two memory banks allow writing of data to a first of said two memory banks simultaneous with reading of data from a second of said two memory banks;

serial communication lines coupled to said input memory and operative to output said parallel output data word onto a parallel data bus;

an output memory operative to receive a parallel input data word from said parallel data bus and to convert said received parallel input data word into a plurality of serial data words, said output memory including a second memory device; and

a serial data output interface for receiving said plurality of serial data words and for providing a serially converted output data word.

29. (previously presented) The converter of claim 28 wherein said input memory comprises:

a serial-to-parallel mapping circuit responsive to said receiving to provide write control signals and write address signals to said first memory device.

30. (currently amended) The converter of claim 28 wherein said input memory comprises:

an output mapping circuit in communication with said first memory device;

a parallel output interface; and

a connection between an output port of said output mapping circuit and an input port of said parallel output interface~~, said connection mapping interconnects between an output port of said output mapping circuit and an input port of said parallel output interface~~.

31. (currently amended) The converter of claim 30 wherein said connection between an output port of said output mapping circuit and an input port of said parallel output interface ~~mapping said interconnects~~ is operative to reorder at least one bit of an output data word from said first memory device to provide said parallel output data word.

32. (previously presented) The converter of claim 28 wherein said second memory device includes two second-memory-device memory banks, which two memory banks allow writing of data to a first of said two second-memory-device memory banks simultaneous with reading of data from a second of said two second-memory-device memory banks.